

APPROVED	O.G. FIG. 2
BY	CLASS. SUB. 35.00
DRAFTSMAN	438 706

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK ETCH  
Inventor: Pan et al.  
Serial No.: 09/614,113  
Docket No.: 2269-2915.3US

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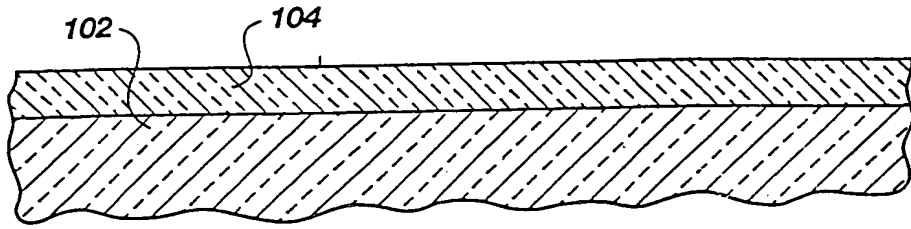


Fig. 1

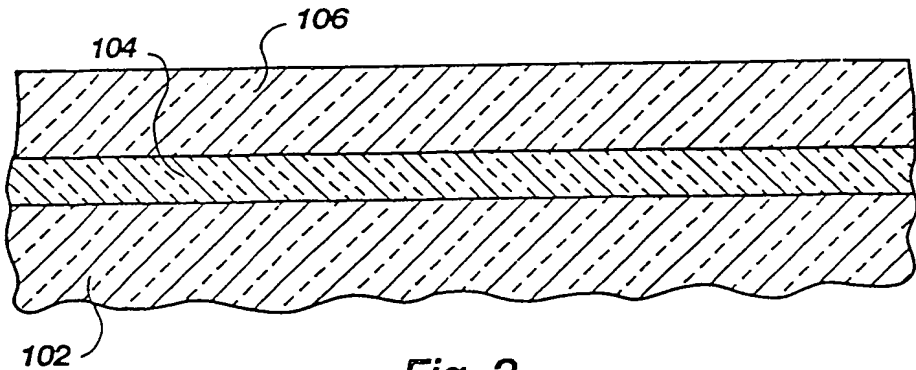


Fig. 2

APPROVED  
DRAFTSMAN  
FEB 24 2003  
PATENT & TRADEMARK OFFICE

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK ETC  
Inventor: Pan et al.  
Serial No.: 09/614,113  
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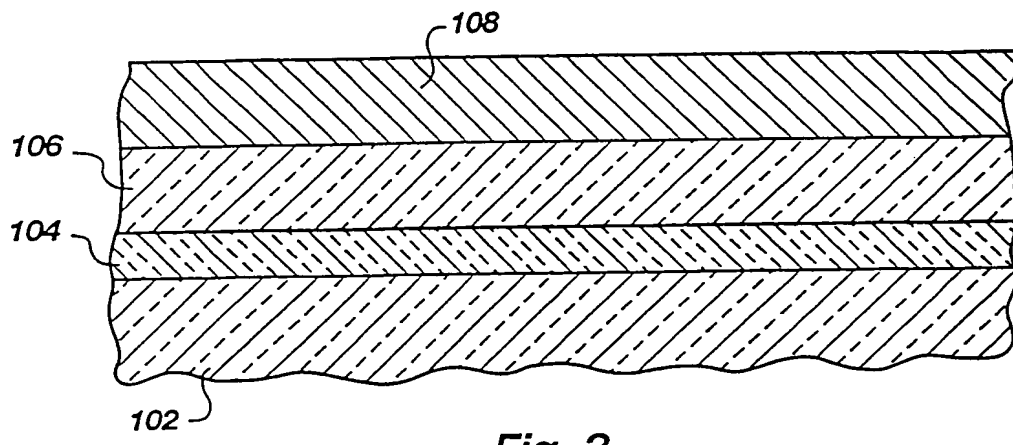


Fig. 3

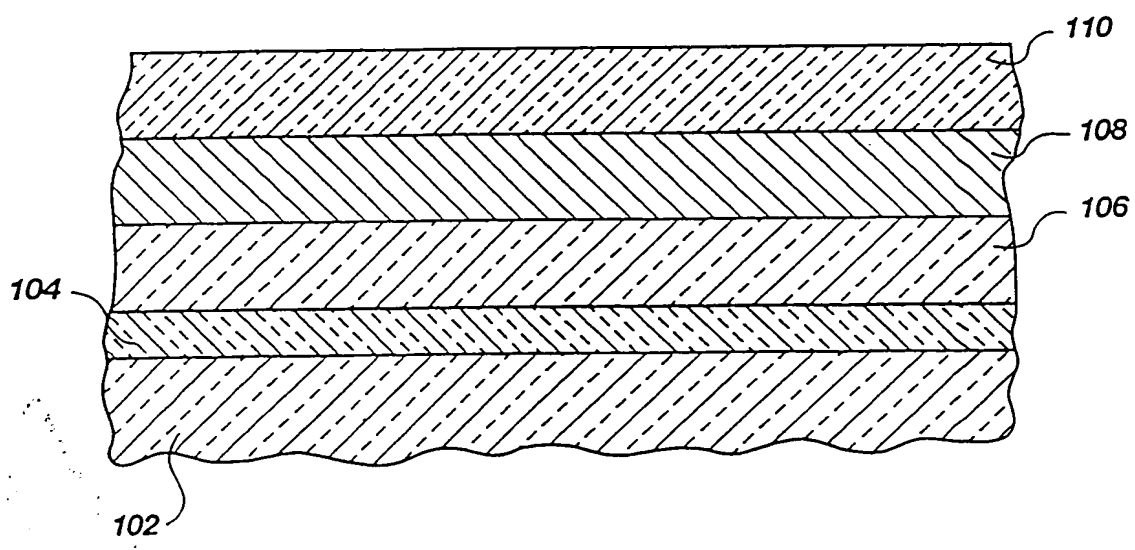
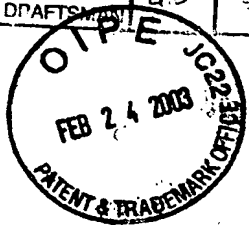


Fig. 4

APPROVED	O.G. FIG. 6	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	708

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK E  
Inventor: Pan et al.  
Serial No.: 09/614,113  
Docket No.: 2269-2915.3US



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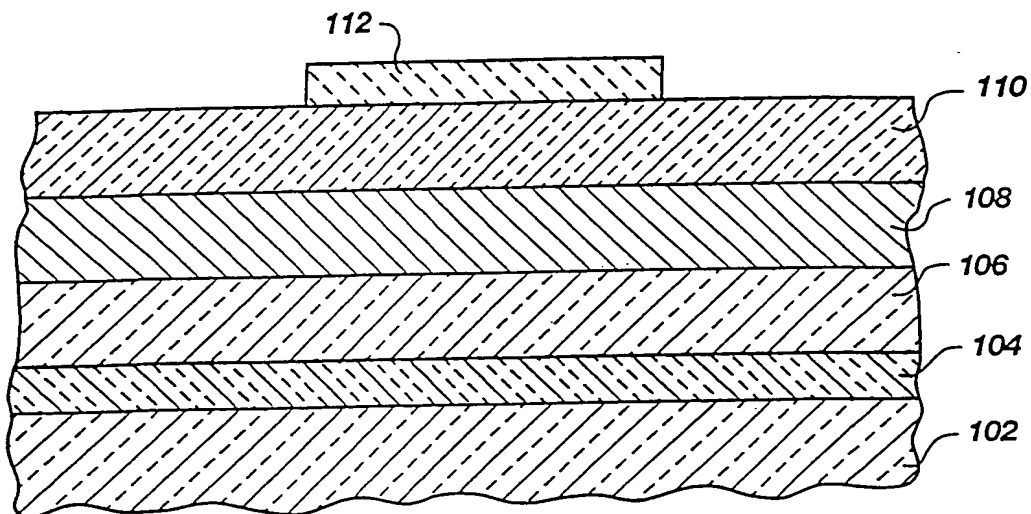


Fig. 5

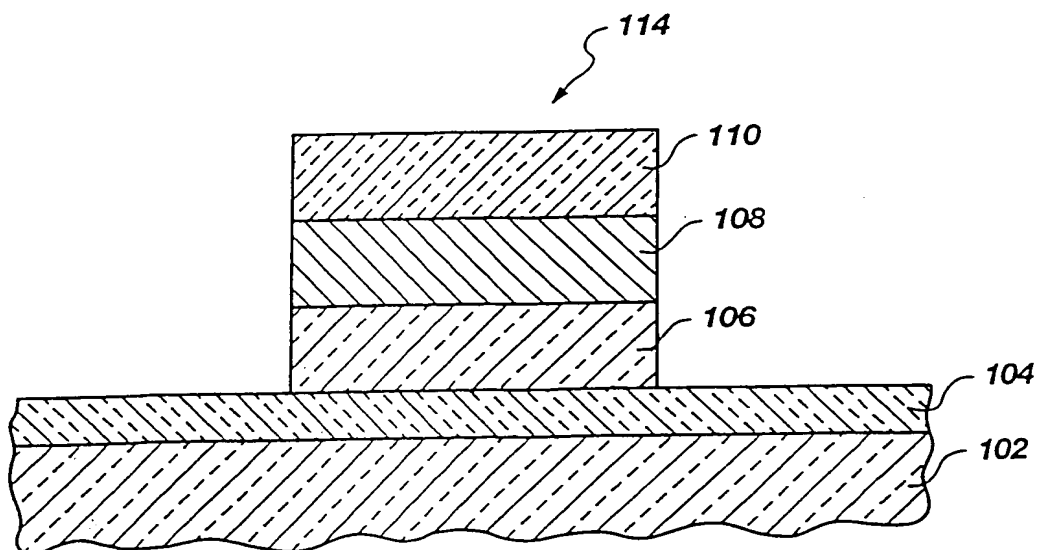
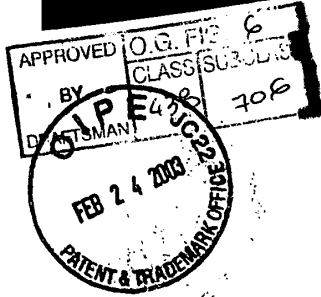


Fig. 6

(24)



TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK ETC  
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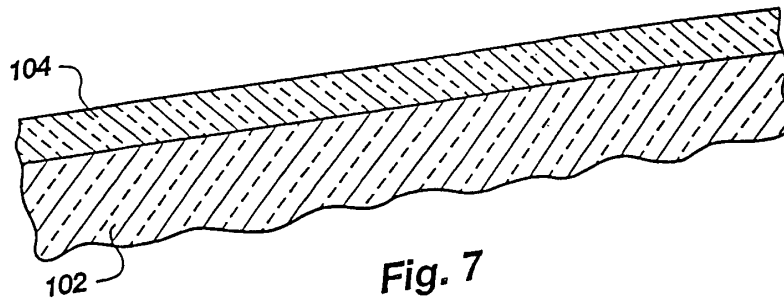


Fig. 7

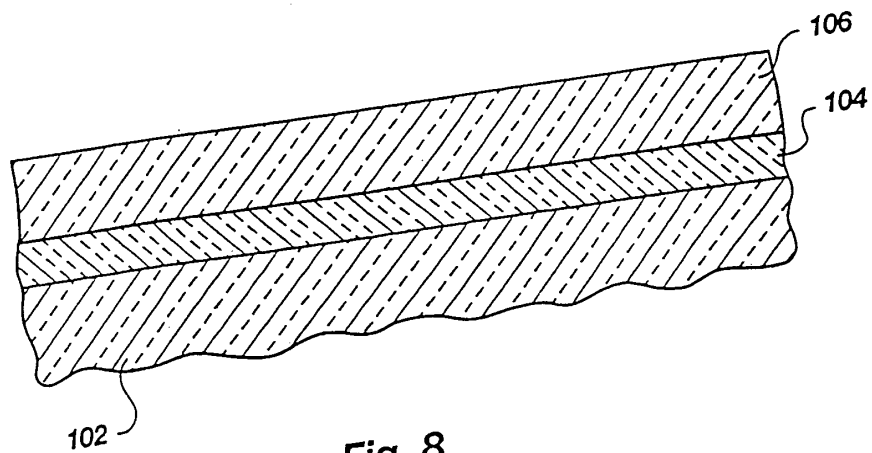


Fig. 8

APPROVED	O.G. FIG. 6
BY	CLASS
DRAFTSMAN	SUBCL/SS
438	708

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK ETC  
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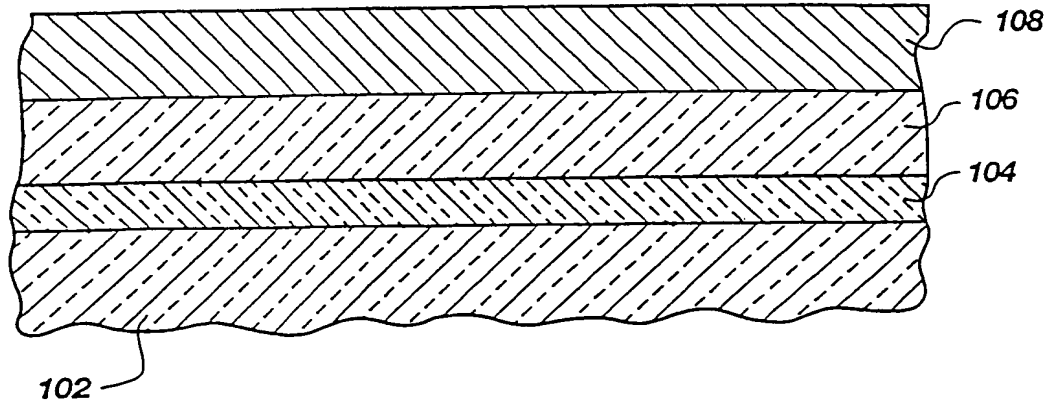
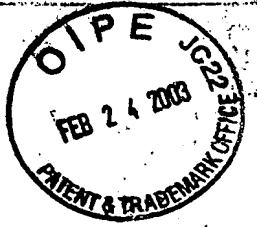


Fig. 9

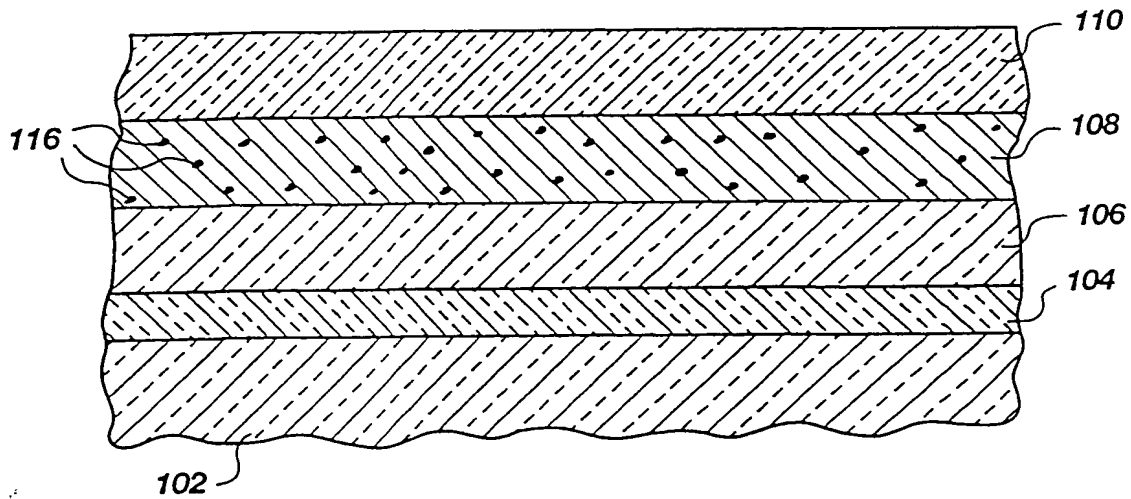


Fig. 10

APPROVED	O.G. FIG. 6
BY	CLASS. SUBCLASS
DRAFTSMAN	438 706

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SUBSTRATE DURING GATE STACK E  
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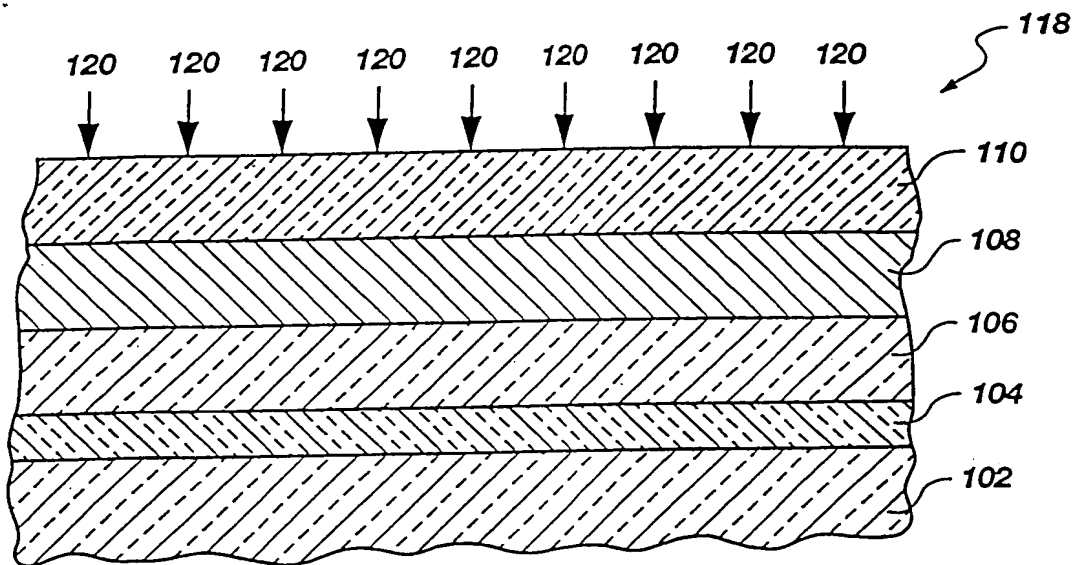


Fig. 11

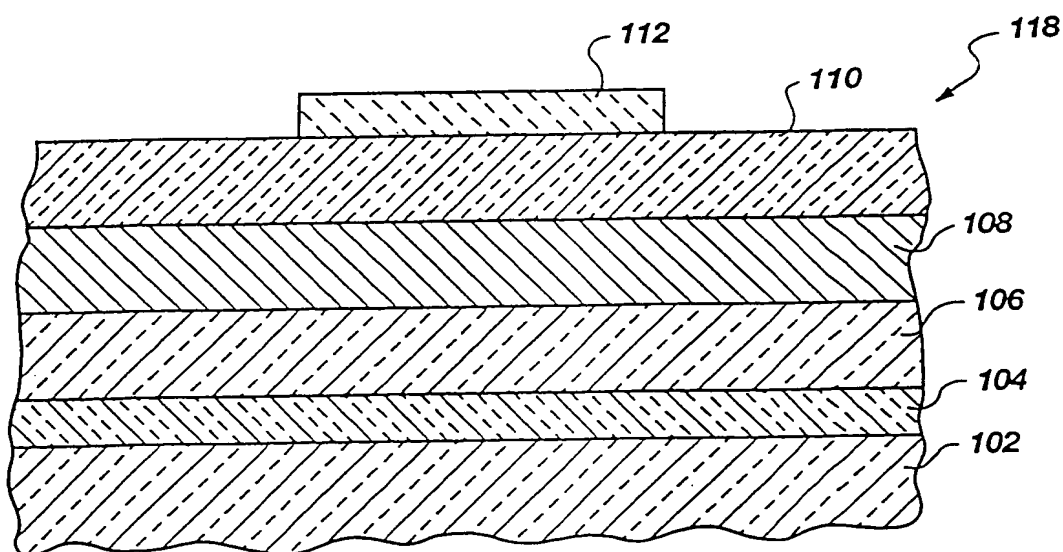
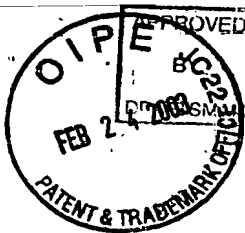


Fig. 12



APPROVED		O.G. FIG.		TITLE	
CLASS	SU	438	706		

TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK

Inventor: Pan et al.  
Serial No.: 09/614,113  
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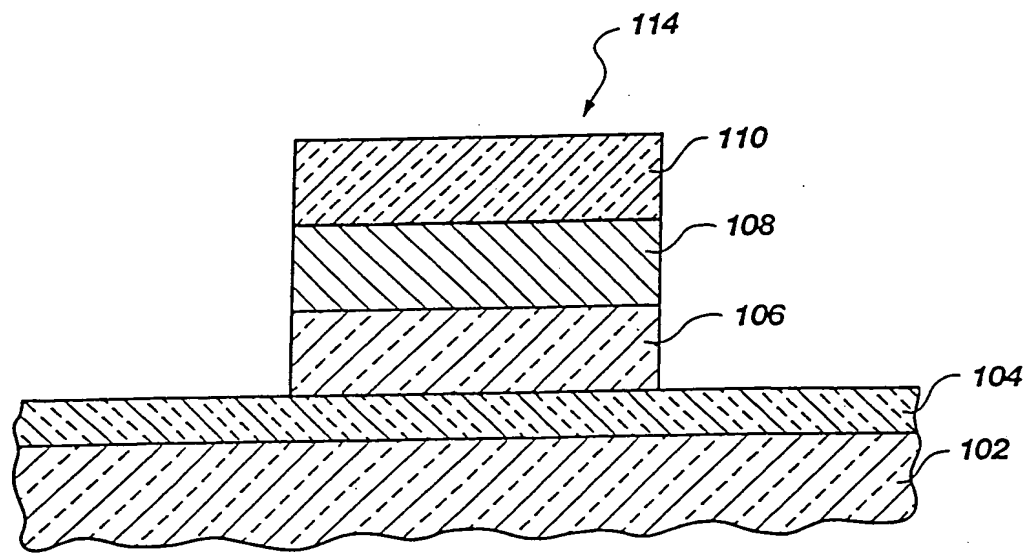
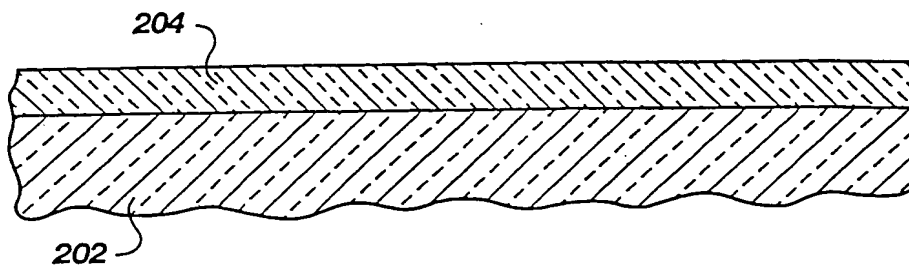


Fig. 13

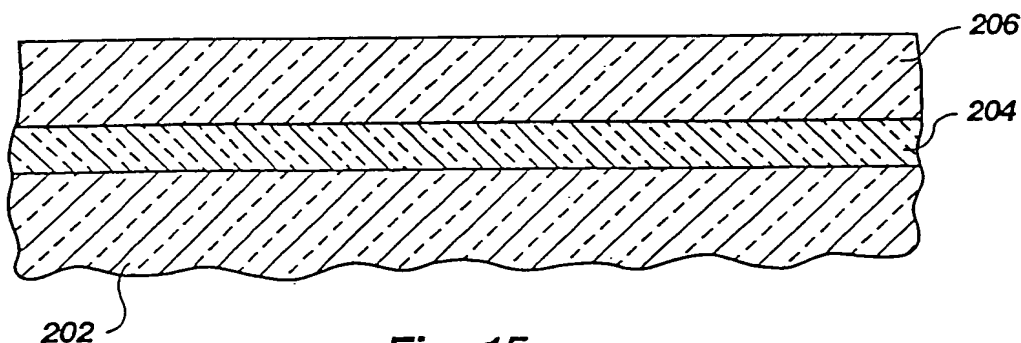
APPROVED	O.G. FILE 6
BY	CLASS/SUBCLASS
DRAFTSMAN	438 706

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
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Inventor: Pan et al.  
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**Fig. 14**  
**(PRIOR ART)**

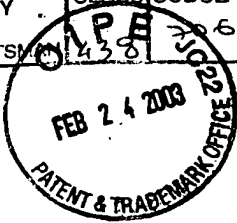


**Fig. 15**  
**(PRIOR ART)**

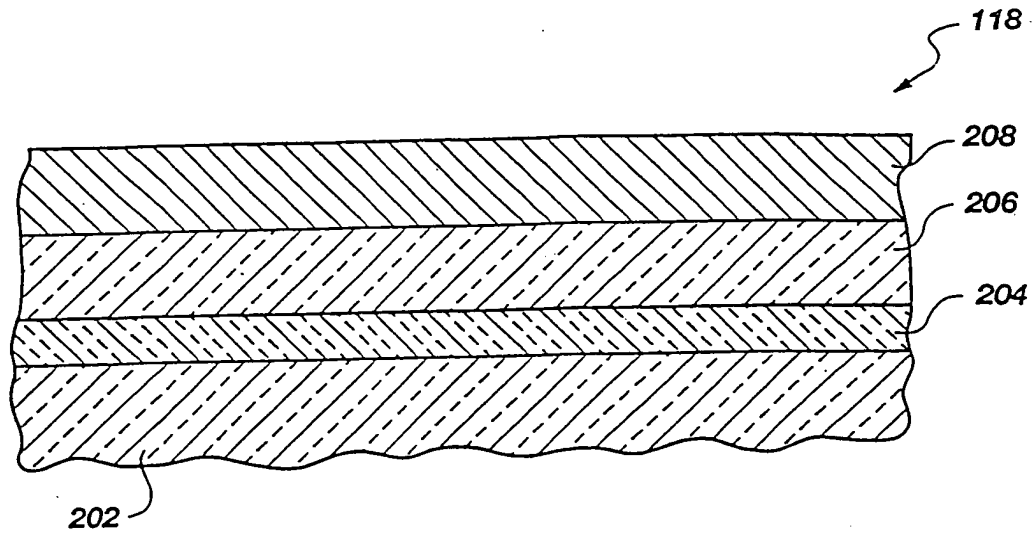


APPROVED	O.G. FIG.
BY	CLASS. SUBCLAS.
DRAFTSMAN	438 306

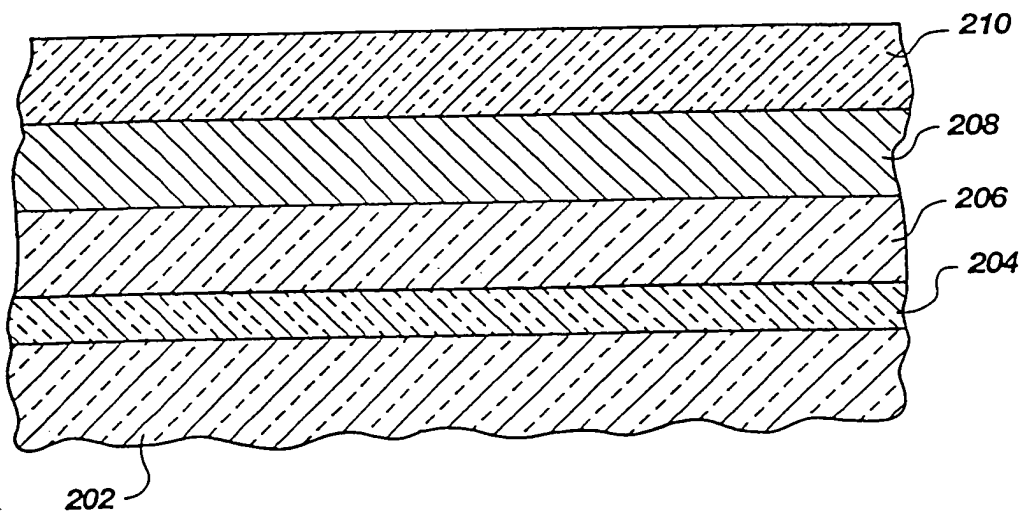
TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK ETC  
Inventor: Pan et al.  
Serial No.: 09/614,113  
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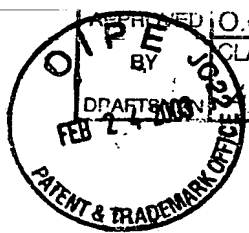
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**Fig. 16**  
(PRIOR ART)



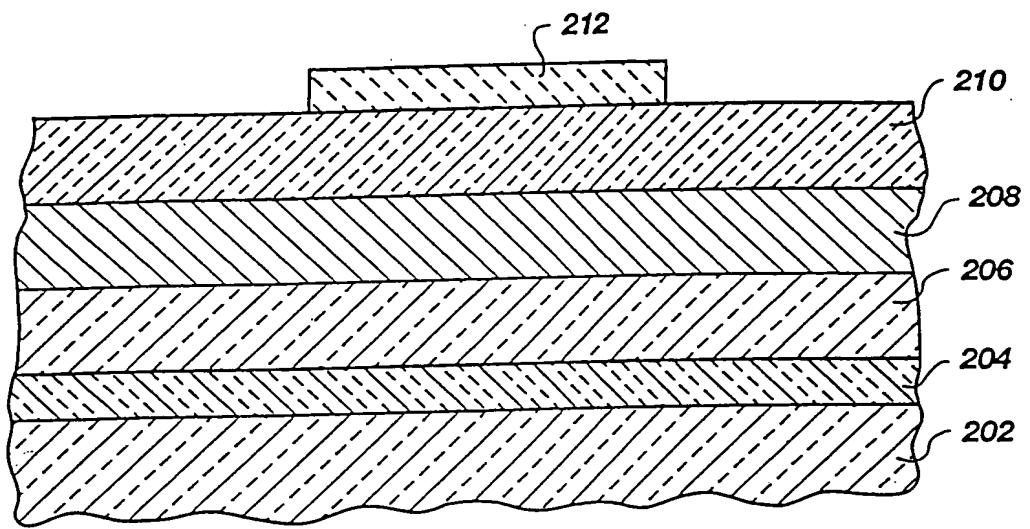
**Fig. 17**  
(PRIOR ART)



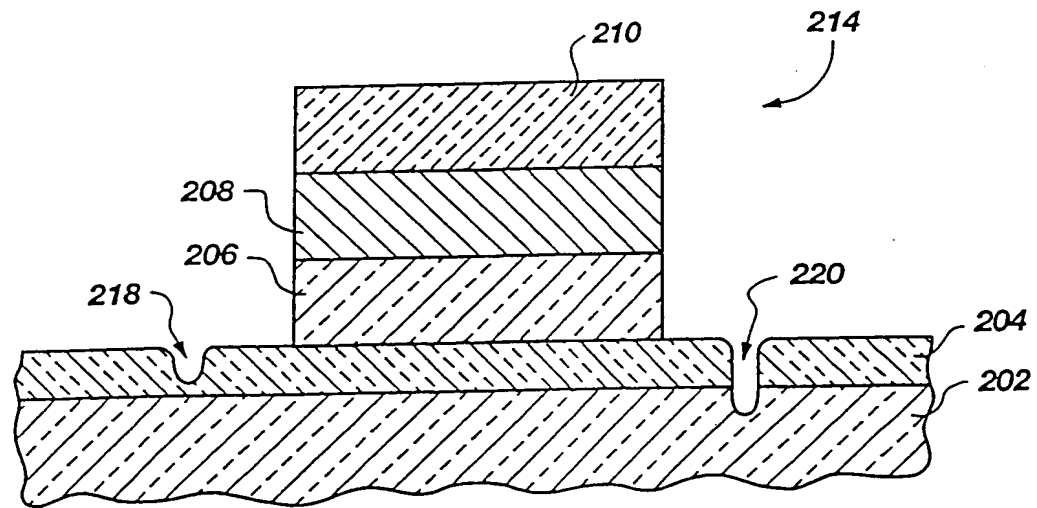
CLASS/SUBCLASS  
38 706

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK ETCH  
Inventor: Pan et al.  
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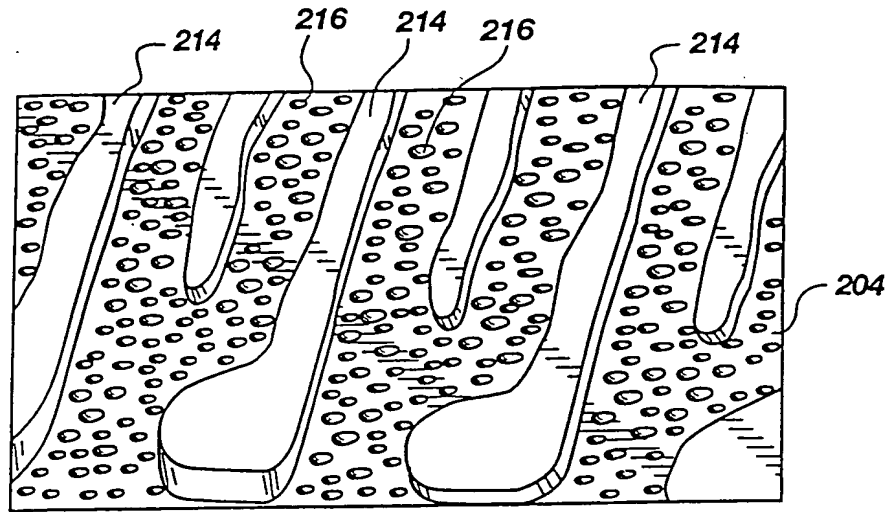
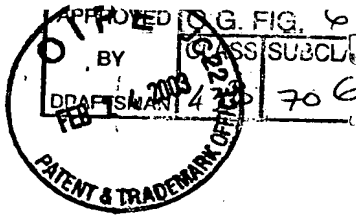
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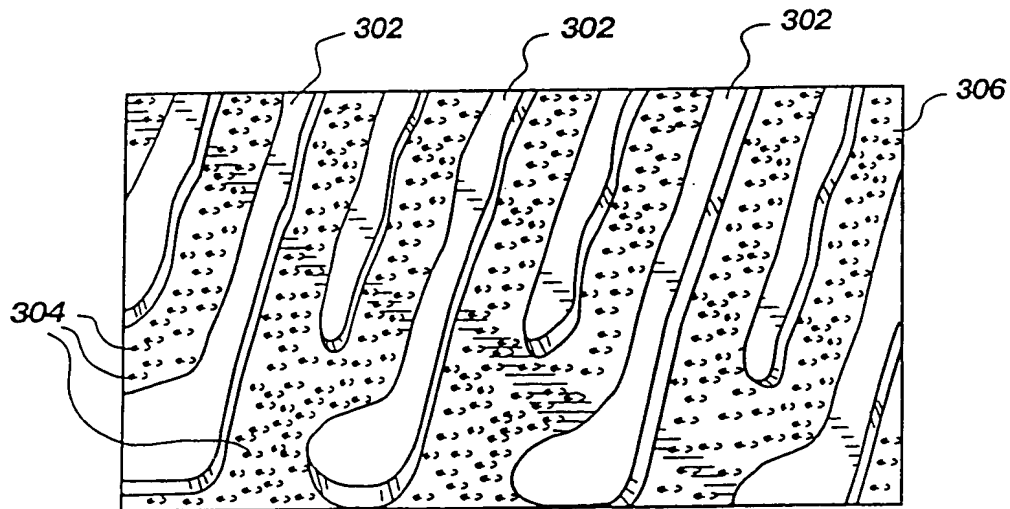
**Fig. 18**  
(PRIOR ART)



**Fig. 19**  
(PRIOR ART)



**Fig. 20**  
(PRIOR ART)



**Fig. 21**  
(PRIOR ART)

APPROVED	O.G. FIG. 8
BY	CLASS SUBCLAS
DRAFT	138 706

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
SUBSTRATE DURING GATE STACK ETC

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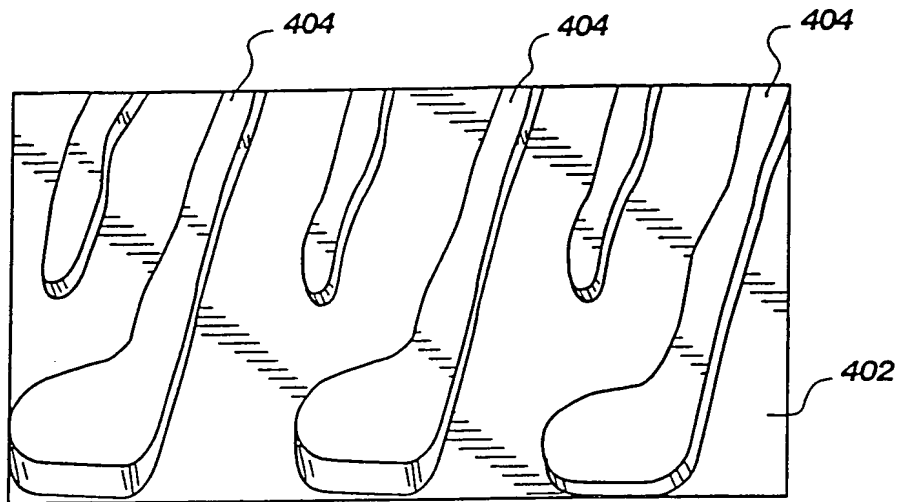


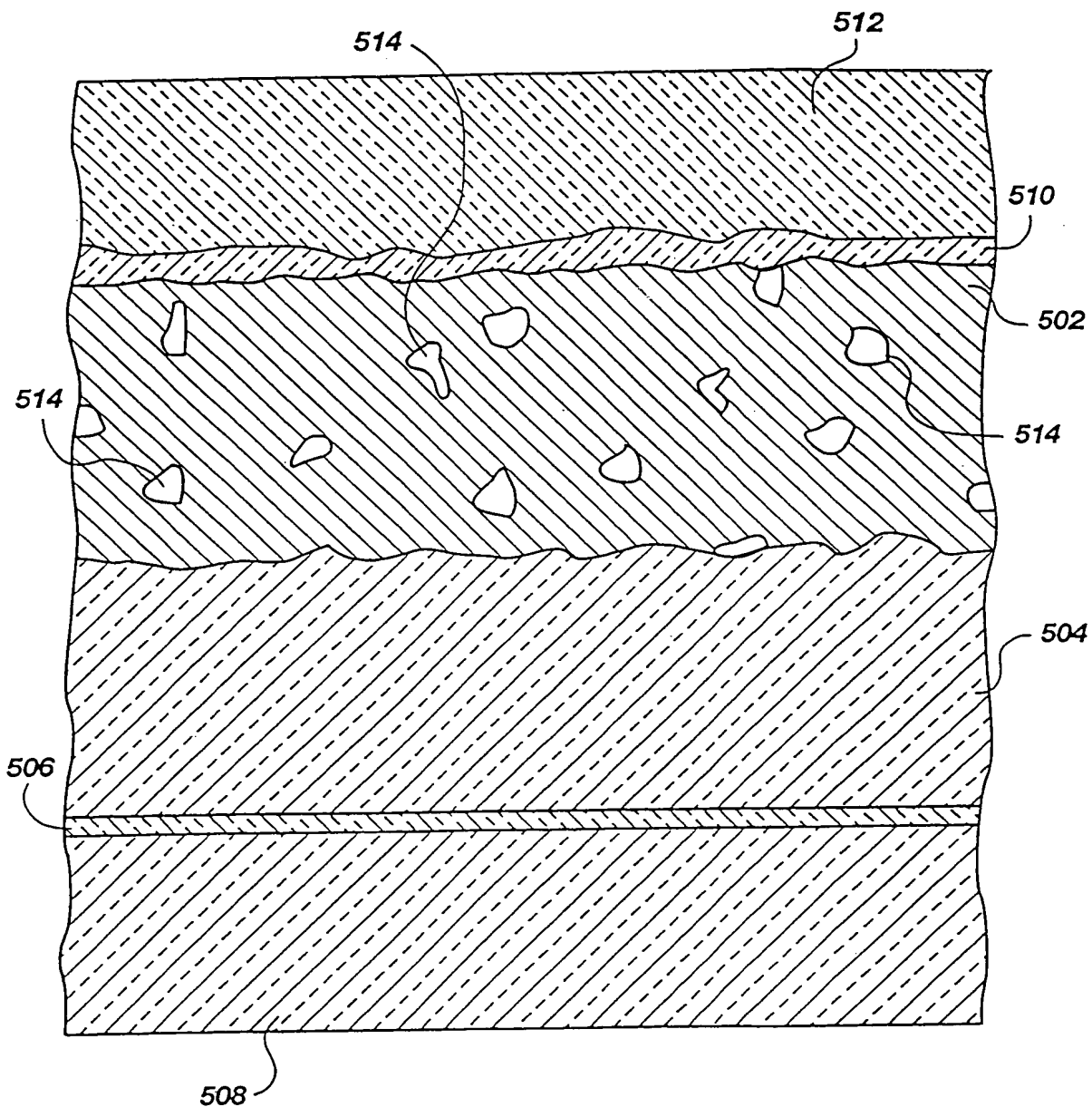
Fig. 22

APPROVED	O.G. FIG. 6	
BY	CLASS	SUBCLASS
DRAFTSMAN	438	706

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**Fig. 23**  
**(PRIOR ART)**

APPROVED	U.G. FIG. 6
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TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON  
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Inventor: Pan et al.  
Serial No.: 09/614,113  
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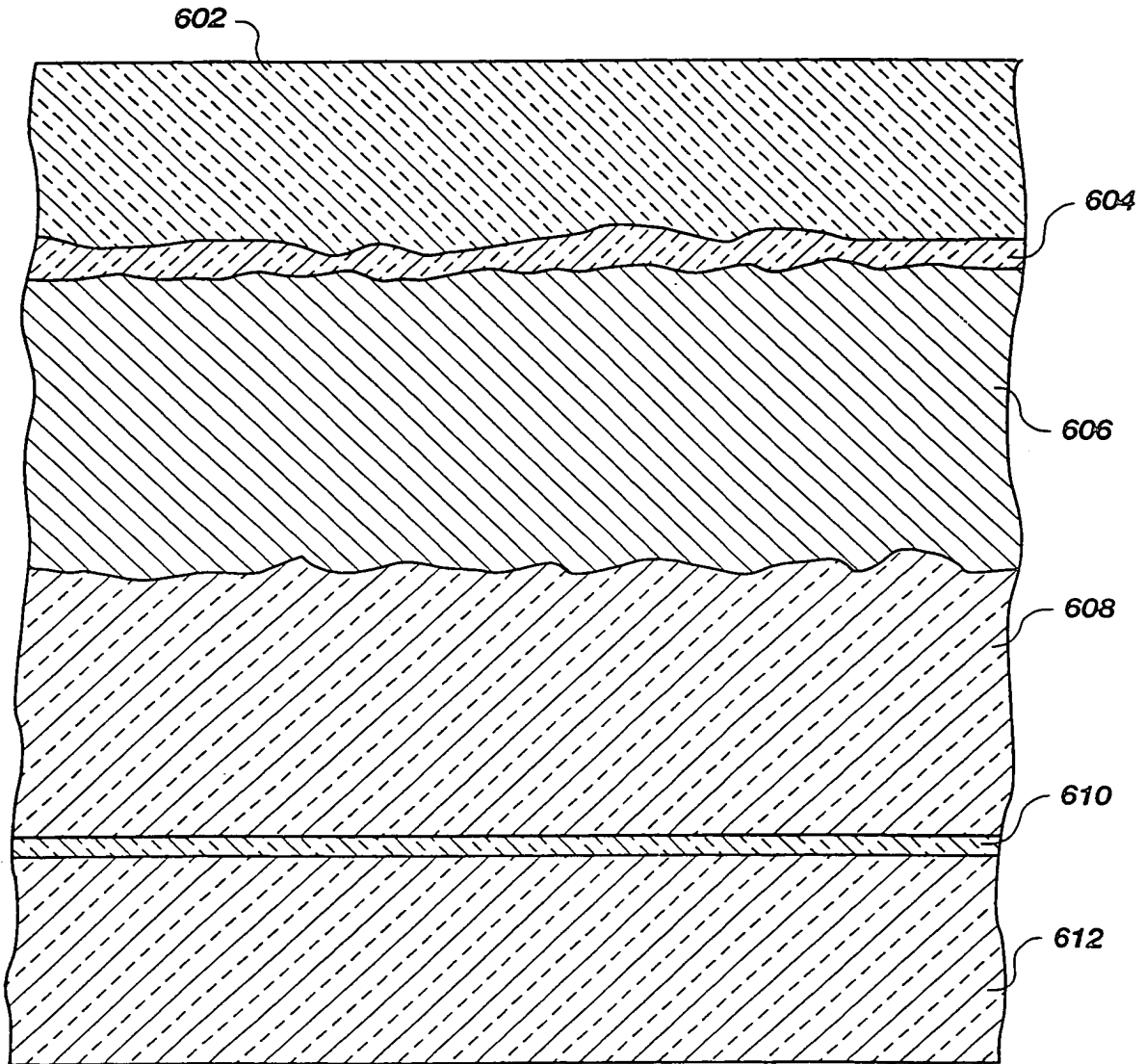
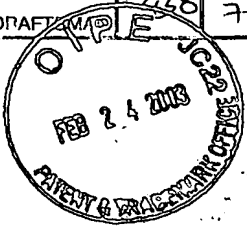


Fig. 24